DRAWING AMENDMENTS

Applicant proposes to amend the drawings by adding the accompanying new sheet containing a proposed new FIG. 4.

REMARKS

Applicant gratefully acknowledges that the finality of the Office Action mailed June 15, 2005, has been withdrawn and that the submission filed on October 11, 2005 has been entered.

The examiner has objected to the amendment that was filed on November 16, 2005 as introducing new matter.

Applicant withdraws the request for entry of the FIG. 4 that was filed on November 16, 2005. The proposed new FIG. 4 that is submitted herewith illustrates schematically the demultiplexer and the system decoder. Applicant believes that the proposed new FIG. 4 does not introduce any new matter and that it provides a helpful framework for the detailed description, particularly the paragraph starting at page 4, line 4. Illustration of the system target decoder in the new FIG. 4 is supported by the description at page 5, line 1, of the specification as originally filed. The proposed FIG. 4 emphasizes, as pointed out by the examiner, that the logical smoothing buffer is distinct from the system target decoder. In accordance with page 2, lines 16-17, FIG. 4 depicts a separate logical smoothing buffer for each SPTS.

Applicant believes that the proposed new FIG. 4 avoids the objection to the previously proposed FIG. 4 and that therefore FIG. 4 should be entered. Withdrawing the request for entry of the previously proposed FIG. 4 and submitting the new FIG. 4 should not be taken as implying that applicant agrees that the previously proposed FIG. 4 contained new matter. Specifically, applicant submits that a decoder buffer and a decoder are inherent in the system target decoder as that term is understood by those skilled in the art.

The examiner has objected to the amendments to the paragraph starting at page 4, line 4, because that paragraph refers to FIG. 4. The examiner has not raised an independent basis for objection to the amendments in question. Since the basis for the examiner's objection to FIG. 4 has been removed, the basis for the objection to the amendments to the paragraph starting at page 4, line 4, has also been removed.

The examiner has also objected to the amendments to the paragraph starting at page 6, line 11. Applicant gratefully acknowledges that the examiner's objection has prompted review of this paragraph and correction of the amendments to refer to Q_j/R_n rather than R_n*Q_j.

The examiner has referred to three bases for objecting to the amendments to the paragraph starting at page 6, line 11:

1. The examiner has objected that Q_j was not previously defined by the specification.

2. The examiner has objected that the sentence "At time δ before DTS_1, frame 1 begins loading into the buffer and continues loading until time $\delta + R_n*Q_1$ before DTS_1." is not supported by the specification.

3. The examiner has objected that the sentence "Since frame 1 has fewer bits than the capacity of one slot, R_n*Q_1 is less than DTS_2-DTS_1 and there is a gap before frame 2 starts loading into the buffer, at time δ before DTS_2." is not supported by the specification based on R_n*Q_1 is less than DTS_2-DTS_1.

Before discussing the examiner's objections in detail, and showing that no new matter has in fact been added, applicant offers four statements regarding what is disclosed in the application as originally filed:

(a) Each frame is loaded into the smoothing buffer at a constant rate R_n bits/s.

(b) The buffer slots are of equal capacity.

(c) The consecutive decode time stamps indicate times that are at equal intervals. Thus, (DTS_{j+1} - DTS_j) is the same for all j. This can be inferred from the fact that the buffer slots are of equal capacity.

(d) Each slot of the buffer has a capacity equal to R_n multiplied by the interval between the times indicated by two consecutive decode time stamps (DTS_{j+1} - DTS_j), i.e. $R_n*(DTS_{j+1}$ - $DTS_j)$.

Applicant will now discuss the new matter objections in detail:

1. The objection that Q_j was not previously defined by the specification could be based either on the contention that the substantive concept of frame size has not been disclosed in the specification as originally filed or on the fact that the specific variable Q_j was not used in the specification as originally filed.

With regard to the first possibility, applicant submits that the concept of frame size has been clearly disclosed in the specification as originally filed and accordingly explicit mention of frame size does not introduce new matter. For example, the paragraph starting at page 6, line 11, of the specification as originally filed states that the buffer may be thought of as having

a plurality of equal capacity slots and that frame 1 has fewer bits than the capacity of one slot in the buffer whereas frame 3 has more bits than fit into one slot. Thus, this paragraph introduces the concept of a measure of the size in bits of a frame relative to the capacity of one slot and shows that the size of frame 1 is less than the capacity of one slot and the size of frame 3 is greater than the capacity of one slot.

With regard to the second possibility, since the concept of frame size is disclosed in the specification as originally filed, defining and using a symbol (Q_j) representing the size in bits of frame j does not introduce new matter. Having introduced j as an appropriate index for a picture or frame, use of the same index in connection with a different variable (frame size as opposed to frame number) does not introduce new matter.

2. The sentence "At time δ before DTS_1, frame 1 begins loading into the buffer and continues loading until time $\delta + R_n*Q_1$ before DTS_1." has been amended to refer to Q_1/R_n. Applicant submits that the sentence, as now amended, does not contain new matter.

The application as originally filed discloses that frame 1 begins loading into the buffer at time δ before DTS_1. See FIG. 3.

The time taken to load a frame of size Q_1 at a rate R_n is equal to Q_1/R_n. It is therefore elementary that frame 1 continues loading until time $\delta + Q_1/R_n$ before DTS_1.

3. The sentence "Since frame 1 has fewer bits than the capacity of one slot, R_n*Q_1 is less than DTS_2-DTS_1 and there is a gap before frame 2 starts loading into the buffer, at time δ before DTS_2." has been corrected to refer to Q_1/R_n instead of R_n*Q_1.

Applicant submits that the statement "Q_1/R_n is less than DTS_2-DTS_1" does not contain new matter because it is precisely what follows from the fact that frame 1 has fewer bits than the capacity of one slot: since the capacity of one slot is equal to $R_n*(DTS_j-DTS_{j-1})$ and Q_1 is less than the capacity of one slot, Q_1/R_n is less than (DTS_2-DTS_1)

The examiner has maintained the rejection on the ground of obviousness over Haskell in view of Zhu et al.

As stated in claim 1, the present invention is concerned with a method of demultiplexing a statistically multiplexed MPEG transport stream into a constant bit rate single program transport stream. A statistically multiplexed MPEG transport stream contains multiple single program transport streams, each composed of a video elementary stream and at least one audio elementary stream.

Applicant takes issue with the following points made by the examiner in support of the rejection of claim 1 under 35 USC 103:

1. The examiner asserts that FIG. 2 of Haskell "discloses demultiplexing VBR streams of data composed of sequences for a picture based on a decode time stamp." Applicant believes that the examiner takes the position that the video data buffer 202 of Haskell corresponds to the smoothing buffer recited in claim 1 and that the block 201 performs the claimed function of "separating a specified single program transport stream...from the statistically multiplexed MPEG transport stream." Applicant agrees with the examiner that Haskell does not disclose that the data received from the data channel by the block 201 is a statistically multiplexed stream and discusses further below why the examiner is incorrect in asserting that a person skilled in the art would consider that the data was a statistically multiplexed MPEG transport stream. Applicant submits, however, that the block 201 does not "separate a specified single program transport stream" from the data received from the data channel. A single program transport stream includes, as noted above, a video elementary stream and at least one audio elementary stream. Haskell might teach that the block 201 separates video data from audio data, and routes the video data and audio data to respective data buffers, but does not disclose or suggest that the block 201 separates a single program transport stream from the input data received by the block 201 and supplies a single program transport stream (video ES and audio ES) to the video data buffer 202.

2. The examiner asserts that "one example of a smoothing buffer is video data buffer 202." In order for the video data buffer 202 of Haskell to be an apt counterpart of the smoothing buffer recited in claim 1, it appears that the examiner must take the position that the video data constitutes the "specified single program transport stream including a variable bit rate program composed of a sequence of pictures." As discussed above, the video data does not constitute a single program transport stream, as that term is understood by those skilled in the art, and applicant submits that even if this interpretation is incorrect and the video data can reasonably be considered to constitute a single program transport stream including a program composed of a sequence of pictures, it is not a variable bit rate program as required by claim 1. The common illustration of idealized operation of a video data buffer supplying a video decoder illustrates fullness of the buffer

by a sawtooth waveform composed of a succession of linear ramp segments, each directed upwards and to the right and each followed by a vertical downward segment, for example as shown in FIG. 8 of Zhu et al. The ramp segments depict increasing fullness of the buffer as data is loaded into the buffer from the channel whereas the vertical downward segments depict the instantaneous decrease in fullness upon removal of data for decoding. The ramp segments are all of uniform slope and are all of equal slope. Accordingly, the data rate is constant. Thus, in the absence of explicit disclosure in Haskell, which applicant believes is absent, applicant submits that a person of ordinary skill in the art would interpret Haskell as disclosing that the video data is supplied at a constant bit rate to the video data buffer 202.

3. The examiner refers to column 5, lines 4-20, of Haskell and applicant believes that this is in connection with the final step of claim 1, namely "transferring the picture from the smoothing buffer at a desired constant bit rate at the time indicated by the picture's decode time stamp for decoding." The paragraph in question states "Video display control 203...then extracts the coded video data for the corresponding image representation from video data buffer 202 and passes it to video decoder 204 for decoding." This passage does not disclose that the video data is passed from the video data buffer to the video decoder at a constant bit rate, as would be required in order to meet the terms of the limitation in claim 1, and the examiner has not referred to any other passage of Haskell as disclosing that the data passes from the video data buffer 202 to the video decoder 204 at constant bit rate. Since the data for the successive pictures would be extracted from the video data buffer at uniform intervals corresponding to the intervals between consecutive decode time stamps (again, see FIG. 8 of Zhu et al), yet the pictures would be of different respective sizes (in bits), the video data would not pass from the video data buffer to the video decoder 204 at a constant bit rate.

4. With respect to the nature of the data delivered over the data channel to the demultiplexer unit 200 of Haskell, the examiner refers to the paragraph at column 1, lines 19-24, which states that an ATM network allows video information to be transmitted with variable bit rate which in turn allows statistical multiplexing of data from a relatively large number of users for transmission over a single data channel. This is the only reference in the entire disclosure of Haskell to statistical multiplexing, and therefore a

person of ordinary skill in the art would not assume that the paragraph has any special relevance to the detailed description. Any inference that the data delivered over the data channel to the demultiplexer unit 200 is statistically multiplexed is based on after-the-fact speculation. Further, although the title of the specification refers to variable bit rate video, the only reference to variable bit rate video in the detailed description is at column 4, lines 4-5, relating to selection of the number of bits to be transmitted for each image representation. In the circumstances, applicant submits that little weight should be accorded to this disclosure.

5. Claim 1 specifies that the loading of a picture into the smoothing buffer commences "a specified amount of time prior to the time indicated by the picture's decode time stamp." The examiner has stated that part of the purpose of the video data buffer 202 of Haskell is to load the buffer early with packets for a frame so that when the frame's decode time comes, the full data for the frame is available for decoding. However, applicant submits that Haskell is deficient with respect to the "specified amount of time prior to the time indicated by the picture's decode time stamp." Haskell does not disclose or suggest that the video data enters the buffer 202 other than as a continuous, constant bit rate stream, as mentioned above, in which case the time at which loading of a picture into the buffer commences will always be immediately after loading of the previous picture ended rather than a specified amount of time prior to the time indicated by the picture's decode time stamp.

6. With respect to claim 3, the examiner points out that the video data is saved in the video decoder buffer of Haskell as soon as it arrives. However, Haskell does not disclose or suggest that this eventuality only occurs "in the event that a picture cannot be loaded into the smoothing buffer the specified amount of time prior to the time indicated by the picture's decode time stamp," as required by claim 3. Thus, as described in the specification, the present invention is concerned with two distinct possibilities: first, when loading of the picture into the smoothing buffer can commence at the time δ prior to the decode time stamp of the picture (because loading of the previous picture has already finished), in which case loading of the picture into the smoothing buffer commences at the time δ prior to the decode time stamp; and second, when loading of the picture into the smoothing buffer cannot start at the time δ prior to the picture's decode time stamp (because the

previous picture has not yet finished loading), in which case the picture is loaded into the smoothing buffer as soon as possible after the time δ prior to the picture's decode time stamp.

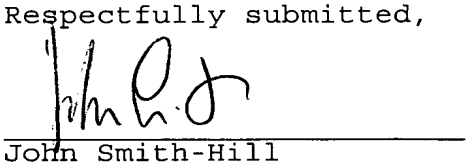
In view of the foregoing, applicant submits that claims 1-3, 6 and 7 are patentable over Haskell and Zhu et al, whether taken singly or in combination.

Claims 10 and 11 have been rejected under 35 USC 112, second paragraph. Applicant respectfully traverses the rejection. The equation referred to by the examiner is not the basis for the features to which the examiner has referred. The features to which the examiner refers are supported by the description at page 6, lines 11-22. As noted at page 6, lines 13-14, the buffer has a plurality of equal capacity slots. The slot for receiving frame 1 is between $DTS_1-\delta$ and $DTS_2-\delta$. In general, the slot for receiving frame j is between $DTS_j-\delta$ and $DTS_{j+1}-\delta$. The goal is to start loading a given picture (the (j+1)'th picture in the context of claim 10) into the smoothing buffer at the time δ before the time indicated by the decode time stamp of that picture. Whether it is possible to meet this goal depends on whether loading of the j'th picture is completed before the desired time to start loading the (j+1)'th picture. Thus, since frame 1 has fewer bits than the capacity of one slot of the buffer, loading of frame 1 into the smoothing buffer is completed no later than the time δ before the time indicated by the decode time stamp of frame 2, and in this case loading of frame 2 into the smoothing buffer starts at the time δ before the time indicated by the decode time stamp of frame 2. Since frame 3 has more bits than fit into one slot, frame 3 continues loading until after $DTS_4-\delta$ and frame 4 is loaded as soon as possible after loading of frame 3 is completed. Applicant therefore submits that the specification as originally filed describes the subject matter of claim 10 in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Applicant submits that the mode of operation defined in claim 10 is not disclosed or suggested by the prior art cited by the examiner. Specifically, the cited references, whether taken singly or in combination, do not disclose or suggest the two rules that are specified in claim 10 regarding when loading of the (j+1)'th picture into the smoothing buffer starts. Accordingly, claims 10 and 11 are patentable.

Applicant has added new claims 12-15. Claim 12 is based on the previous claim 4 but recites in greater detail (similarly to claim 10) the conditions determining when loading of the j'th picture into the smoothing buffer starts. Claim 12 is allowable for the reasons presented in support of claim 10. It therefore follows that claim 12 and the dependent claims 13-15 are patentable.

Respectfully submitted,



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